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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,962	12/21/2006	Reinhard Weiberle	10191/4593	2381

26646 7590 10/06/2009

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EXAMINER	
TREAT, WILLIAM M	
ART UNIT	PAPER NUMBER
2181	
MAIL DATE	DELIVERY MODE
10/06/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/560,962	WEIBERLE ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 29-58 are presented for examination.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 29-58 rejected under 35 U.S.C. 103(a) as being unpatentable over Grochowski et al. (Patent No. 6,615,366) in view of Moughanni et al. (Patent No. 6,003,133).

5. Grochowski taught the invention of exemplary claim 29 including: “a processor system (Fig. 2A), comprising: at least two execution units (110(a), 110(b)); a memory (270); and a switch-over unit for switching between at least two operating modes of the processor system (col. 3, lines 30-67). In the cited material Grochowski describes operating in what he terms a high reliability (HR) mode operating system code and critical applications which operate directly on the platform hardware. For user

applications which are significantly less likely to crash the computer system or threaten its integrity, Grochowski operates in a high performance (HP) mode. Grochowski does not specifically state in the cited section that the code for these two modes is assigned to separate memory regions nor that transitioning between the two regions is done by accessing a predefined memory address.

6. However, Moughanni taught it is conventional to separate operating system and critical applications into a supervisory memory region separate from the user applications in the user region (Fig. 2, col. 3, lines 4-24). Moughanni also taught the interface between these two modes/regions is well defined. He also taught the user/supervisor interface typically consists of interrupts, system calls, reset, and exceptions (col. 3, lines 24-33). These types of transitions between the two modes/regions all take place by accessing a predefined memory address.

7. As to claim 30, Grochowski taught: “the processor system as recited in Claim 29, further comprising: a comparator unit (130), wherein the first operating mode corresponds to a safety mode in which the two execution units redundantly process the same program, and the comparator compares statuses of the two execution units resulting from processing of the same program to determine whether the statuses agree (col. 2, lines 45-53).

8. As to claim 31, Grochowski taught: “the processor system as recited in Claim 30, wherein the two execution units synchronously process the same program in the first operating mode (col. 3, lines 58-60).

9. As to claims 32, 33, and 35, they merely say memory is divided in some unspecified way (i.e., logically(?) or physically(?) or by address(?), etc.) and that when operating in safety/HR mode one only wants to be running code from the safety/HR region of memory and in the performance/HP mode one wants to be running code from the performance/HR region of memory. Gorchowski taught logical regions/divisions such as operating system kernel, code that operates platform hardware, code for color or location of pixels, and code for values in database fields (col. 3, lines 37-50) which would meet the limitations set forth in claims 32, 33, and 35. Also, for Grochowski's invention to work as described, his system must inherently run, when operating in safety/HR mode, code from the safety/HR region of memory, and in the performance/HP mode, code from the performance/HP region of memory.

10. As to claim 40, Grochowski taught: "the processor system as recited in Claim 30, wherein the comparator is switched off in response to the transition into the second operating mode, and wherein the second operating mode is a performance mode, and wherein a comparison of the statuses of the two execution units takes place only in the first operating mode" (col. 2, lines 45-47).

11. As to claims 44-46, 48-51, and 53, they fail to teach or define over rejected claims 29-33, 35, and 40.

12. As to claims 54 and 55, these are merely claims saying that some aspect of the system monitors whether HR code is being incorrectly run when HP code is being run. Inherently, this is being done in Grochowski's system or the purpose of the two modes would be voided.

13. The examiner takes Official Notice of the fact that in claims 34, 36, 41-43, 52, and 56 applicants are merely using conventional techniques related to change-of-flow instructions and concepts used with forms of memory such as protected memory and user memory.

14. MPEP 2144.03 C states that "If applicant does not traverse the examiner's assertion of official notice or applicant's traverse is inadequate the examiner should clearly indicate in the next office action that the common knowledge or well-known in the art statement is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of Official Notice or that the traverse was inadequate. If the traverse was inadequate, the examiner should include an explanation as to why it was inadequate."

15. Applicants did not traverse the examiner's "Official Notice of the fact that in claims 34, 36, 41-43, 52, and 56 applicants are merely using conventional techniques related to change-of-flow instructions and concepts used with forms of memory such as protected memory and user memory." The examiner is now informing applicants that his Official Notice is now admitted prior art.

16. Grochowski makes clear that transitioning from safety/HR mode to performance/HP mode and vice versa requires significant housekeeping operations (col. 4, lines 62-67) which must be undertaken and completed before a given mode is fully operational. In the case of transition from performance/HP mode to safety/HR mode applicants are using an interrupt as might occur when a driver hits the brakes in a panic stop and requires immediate activation of the anti-lock braking system (ABS).

Using interrupts to transition a system from user mode to supervisory mode (the supervisory mode being where tasks critical to the basic computer system are performed) is a conventional technique in the art. Housekeeping related to the transition is done in conjunction with the change of flow, too. Depending on processor design, interrupts can be directly executed in hardware and can also be prioritized which makes them excellent choices for the transition from performance/HP mode to safety/HR mode when critical tasks are involved.

17. On the return to performance/HP mode from safety/HR mode it is unclear from applicants' disclosure whether applicants use a return instruction or some other form of change of flow instruction but the techniques are familiar. As with a return from an interrupt, there will be housekeeping tasks. Applicants' system must either recognize the address of the instruction to be executed as that of a change of flow instruction which returns to the performance/HP mode or must examine the address to which the change of flow instruction is redirecting the processor in order to be sure proper housekeeping is done. This is the same type of check necessary when transitioning from supervisory mode to user mode after an interrupt (i.e., the system must know when to restore the program state for the interrupted program, where to resume execution of and fetching of instructions, etc.). Modern processors prefetch their instructions and instruction operands, too, because of the disparity between processor and memory speeds allowing for lookahead examination of addresses of instructions and of their operands. This prevents a prolonged stall when something as complex as a transition from one mode of operation to another is performed.

18. Applicants' use of interrupts, change of flow instructions, and lookahead recognition of addresses to transition from one mode to another merely represents the application of known techniques in the art to bring about expected results. For the reasons stated claims 34, 36, 41-43, 52, and 56 are rejected.

19. Applicants did not traverse the examiner's statement that "use of interrupts, change of flow instructions, and lookahead recognition of addresses to transition from one mode to another merely represents the application of known techniques in the art." The examiner is now informing applicants that this statement about known prior art is now admitted prior art.

20. As to claims 37-38, Grochowski inherently taught some aspect of his system prevented the execution cores which are operating synchronously from erroneously executing code other than safety/HR code while in safety/HR mode or his invention would not work as described in his patent. By the same token, Grochowski inherently taught some aspect of his system prevented the execution cores which are operating asynchronously from erroneously executing code other than performance/HP code while in performance/HP mode or his invention would not work as described in his patent. However, Grochowski did not teach a switch-over unit assigned to the monitoring of this function. But, Grochowski did teach an embodiment with hardware devoted to switching the processor between modes based on memory area which inherently means a memory address or memory addresses. The examiner takes Official Notice, too, that a conventional way to monitor addresses is by comparators. Since Grochowski's switching hardware unit would be monitoring addresses and/or

address lines accessed by the two processors, it would be logical that the system component which monitors addresses which cause a transition from one mode to another could also be used to make certain one or more of the processors did not stray outside the code boundaries of the particular mode.

21. As to claim 47, providing redundant storage of the safety critical program can mean better survivability of the system given some form of catastrophic failure of a portion of memory and can reduce memory contention given sufficient ports and bus lines, but as pointed out in applicants' specification, error correction code is another design option which can save on cost of memory, bus lines, etc.

22. As to claim 39, having separate memory modules for the one version of the performance/HP code and the two copies of the safety/HR code is a design choice which promotes system survivability and potentially reduces resource contention while adding additional hardware cost for redundancy in memory, busses, control structures, etc. Logically, it is a valid design choice one of ordinary skill could readily recognize and implement.

23. As to claims 57-58, they fail to teach or define over rejected claims 29-56.

24. Applicant's arguments filed 9/18/2009 have been fully considered but they are not persuasive.

25. Applicants' have argued in substance that independent claims 29 and 44 and their dependent claims are allowable because (a) "It is therefore not understood as to how or why this references (i.e., Moughanni) suggest to a person skilled in the art the feature in which 'at least one program memory region is exclusively assigned to a first

one of the [at] least two operating modes and at least a second program memory region is exclusively assigned to a second one of the at least two operating mode[s]' "; (b) "Further this reference (i.e., Moughanni) concerns a system having only one CPU. There is no reason why a person skilled in the art would expect to find any useful information in this reference with respect to the operation of a multi-core system, as provided for in the context of the presently claimed subject matter"; and (c) "As to the 'Grochowski' reference, it does not cure these deficiencies of the 'Moughanni' reference". Applicants have argued in substance on behalf of claims 29 and 56 that (d) they are belatedly saying they are traversing the examiner's Official Notice and think it incumbent upon him to provide a reference related to the Official Notice or claims 29 and 56 should be allowable in the absence of such a reference. Applicants' have argued in substance on behalf of new claims 57 and 58 (e) " The 'Grochowski' and 'Moughanni' references, whether taken alone or combined, do not disclose -- and are not asserted to disclose (nor even suggest) - the feature in which at least one first program memory region is exclusively assigned to a first one of the at least two operating modes, and at least one second program memory region is exclusively assigned to a second one of the at least two operating modes, and wherein the at least two execution units are permitted to access the at least one first program memory region only in the first operating mode and the at least one second program memory region only in the second operating mode, as provided for in the context of the presently claimed subject matter."

26. As to 24(a), (b), and (c), the examiner pointed out earlier: "Grochowski taught the invention of exemplary claim 29 including: "a processor system (Fig. 2A), comprising: at least two execution units (110(a), 110(b)); a memory (270); and a switch-over unit for switching between at least two operating modes of the processor system (col. 3, lines 30-67). In the cited material Grochowski describes operating in what he terms a high reliability (HR) mode operating system code and critical applications which operate directly on the platform hardware. For user applications which are significantly less likely to crash the computer system or threaten its integrity, Grochowski operates in a high performance (HP) mode." The examiner also pointed out earlier: "Moughanni taught it is conventional to separate operating system and critical applications into a supervisory memory region separate from the user applications in the user region (Fig. 2, col. 3, lines 4-24)." In the cited section Moughanni explains the operating system and protected system resources such as initializing clocks, initializing peripherals, exception handling, memory mapping, and allocation of resources (i.e., what Growchowski terms critical applications which operate directly on the platform hardware) operate in supervisory or privileged mode in supervisory space. Moughanni also explains user applications (which Growchowski describes as significantly less likely to crash the computer system or threaten its integrity) are run in user space. In KSR the Supreme Court stated: "When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one

device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his ordinary skill. *KSR*, 550 U.S. at, 82 USPQ2d at 1396. When considering obviousness of a combination of known elements, the operative question is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id*. at__82 USPQ2d at 1396." It makes no logical sense to fragment the operating system, critical routines, and user applications and then intermingle those fragments, as applicants seem to be arguing. With such a design, faulty or compromised application code can, by merely incrementing the program counter (PC), fall into critical code that compromises the integrity of the whole system. Instead of a simple comparison mechanism for testing a range, one is forced to establish a table of dynamic ranges of code to determine when one is in one mode or another and to guard against transition from one area to another. Instead of contiguous code being fetched one now has to hop around in memory. Applicants fail to supply any reasoning as to why one would want to implement such an inefficient and dangerous design in a processor with two execution units that concerns itself with the integrity of its critical code and overall system. Also, applicants offer no explanation of technical difficulty that would prevent partitioning the memory of the single-chip, dual-core system of Growchowski in the same manner as the single-chip, single-core processor of Moughanni.

27. AS to 24(d), the examiner gave applicants adequate warning in his first action "that since the KSR decision by the Supreme Court examiners are asked by the Office

to require applicants to provide persuasive evidence and/or persuasive arguments, etc. which clearly contradict the examiner's Official Notice before the examiner provides a reference supporting his position." The examiner in his next action pointed applicants to the appropriate section of the MPEP (MPEP 2144.03 C) where it makes clear what constitutes an adequate traversal of the examiner's Official Notice and that only after such an adequate traversal is the examiner expected to provide a reference.

28. As to 24(e), if the dual-core chip of Grochowski is operating in high reliability (HR) mode which is defined by Growchowski as "the processor operates the execution cores in lock step on identical code segments and compares the results to identify errors (col. 3, lines 58-60)", neither core could be in high performance (HP) mode or the two processors wouldn't be in lock-step and executing HR code from HR memory. If the individual cores of the dual-core chip of Grochowski are operating in HP mode then they are by definition not executing HR code (col. 3, lines 30-35) and, therefore, are not in HR memory but must be in HP memory.

29. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

30. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/William M. Treat/

Primary Examiner, Art Unit 2181